Sanjay Ghodawat University, Kolhapur 2018-19

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Year and Program: 2018-19 F.Y. M. Tech. | **School of Technology** | **Department of Electronics Engineering**

Course Code: EES5082 | **Course Title: Communication Network Processors** | **Semester – II**

Day and Date: Monday 27/05/2019 | **End Semester Examination (ESE)** | **Time:** **Max Marks: 100**

2:30 to 5:30 pm.

Instructions:
1) All questions are compulsory.
2) Assume suitable data wherever necessary.
3) Figures to the right indicate full marks.

			Marks	Bloom's Level	CO
Q.1		**Attempt the following**			
	a)	If the Receiver uses CRC for error detection, examine whether the message M(x) with the generator polynomial P(x) will be accepted or rejected? $P(x) = 1\,1\,0\,0\,1\,1$ & $M(x) = x^4 + x^3 + 1$	7	L_4	CO1
	b)	With the help of block diagram explain the working of STREAM architecture? State its advantages.	7	L_2	CO2
		OR			
	b)	Compare & contrast processes versus tasks.	7	L_5	CO2
Q.2		**Attempt the following**			
	a)	Illustrate, how the inefficiency of the multiple decrements is addressed by a differential timeout scheme?	7	L_3	CO3
		OR			
	a)	With the help of neat diagram explain the STREAMS buffer scheme in details.	7	L_3	CO3
	b)	Illustrate different components of multiboard systems? List the functions of Line card & control card.	7	L_4	CO4
Q.3		**Attempt any two of the following**			
	a)	With the help of neat diagram explain the RS232 DB9S interface used for serial communication.	6	L_2	CO1
	b)	Classify different architectures used for communication equipment's. Explain any one in details.	6	L_3	CO4

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	c)	Describe the options available for accessing the variables in distributed environment?	6	L_2	CO4
Q.4		**Attempt any Two of the following**			
	a)	What are the applicability issues of using PFair scheduling algorithms for packet processing routers.	9	L_2	CO5
	b)	Illustrate with the help of example, the PD^2 tie breaks algorithm.	9	L_3	CO5
	c)	Discuss on how flow gating is used for packet handling in TRIBE architecture.	9	L_3	CO6
Q.5		**Attempt any Two of the following**			
	a)	Explain how the processor scheduling is done using pipelined approach	9	L_2	CO5
	b)	With the help of neat diagram explain the fiber channel to infiniband protocol converter.	9	L_2	CO5
	c)	Sketch the block diagram of massively multithreaded processor(Porthos). Explain the architecture in details	9	L_3	CO5
Q.6		**Attempt any Three of the following**			
	a)	What do you understand by thread migration? Explain how it is done in TRIBE architecture.	8	L_3	CO6
	b)	With the help of neat diagram explain the ASR 1000 series router architecture.	8	L_3	CO6
	c)	With the help of neat diagram explain the packet path through ESP.	8	L_3	CO6
	d)	Enlist the processes handled by RP1 in ASR 1000 router?	8	L_2	CO6

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